EE105 – Fall 2014
Microelectronic Devices and Circuits

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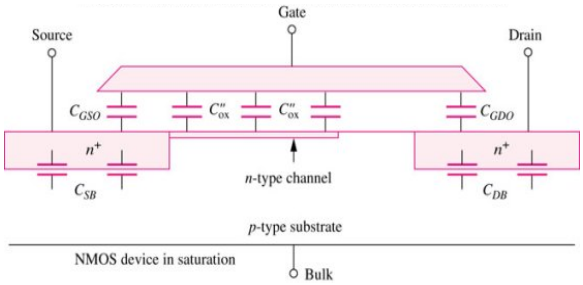
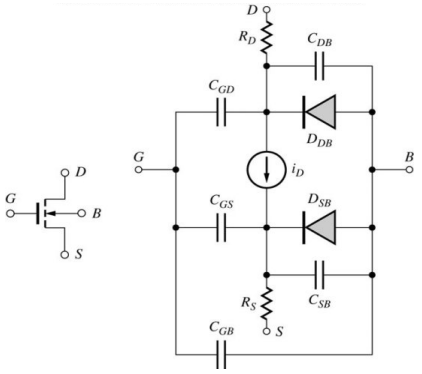
NMOS Transistor Capacitances: Saturation Region



- **Drain no longer connected to channel**

$$C_{GS} = \frac{2}{3}C_{GC} + C_{GSO}W \qquad C_{GD} = C_{GDO}W$$

SPICE Model for NMOS Transistor



Typical default values used by SPICE:

$K_P = 50$ or $20\ \mu A/V^2$

$\gamma = 0$

$\lambda = 0$

$V_{TO} = 1$ V

μ_n or $\mu_p = 500$ or 200 cm^2/V-s

$2\Phi_F = 0.6$ V

$C_{GDO} = C_{GSO} = C_{GBO} = C_{JSW} = 0$

$T_{ox} = 100$ nm

MOS Transistor Scaling

- All physical dimensions shrinks by a factor of α
- All voltages (including threshold voltage) reduced by α also
  - Constant field scaling
- Drain current: $$i_D^* = \mu_n \frac{\varepsilon_{ox}}{T_{ox}/\alpha}\frac{W/\alpha}{L/\alpha}\left(\frac{v_{GS}}{\alpha} - \frac{V_{TN}}{\alpha} - \frac{v_{DS}}{2\alpha}\right)\frac{v_{DS}}{2\alpha} = \frac{i_D}{\alpha}$$
- Gate Capacitance: $$C_{GC}^* = \left(C_{ox}^{"}\right)^* W^* L^* = \frac{\varepsilon_{ox}}{T_{ox}/\alpha}\left(\frac{W}{\alpha}\right)\left(\frac{L}{\alpha}\right) = \frac{C_{GC}}{\alpha}$$
- Circuit delay in a logic circuit.

$$\tau^* = C_{GC}^* \frac{\Delta V^*}{i_D^*} = \frac{C_{GC}}{\alpha}\frac{\Delta V/\alpha}{i_D/\alpha} = \frac{\tau}{\alpha}$$

MOS Transistor Scaling
Scale Factor α (cont.)

- **Circuit and Power Densities:**

$$P^* = V_{DD}^* i_D^* = \frac{V_{DD}}{\alpha}\frac{i_D}{\alpha} = \frac{P}{\alpha^2}$$

$$\frac{P^*}{A^*} = \frac{P^*}{W^* L^*} = \frac{P/\alpha^2}{(W/\alpha)(L/\alpha)} = \frac{P}{A}$$

extremely important result!

- **Power-Delay Product:**

$$PDP^* = P^* \tau^* = \frac{P}{\alpha^2}\frac{\tau}{\alpha} = \frac{PDP}{\alpha^3}$$

- **Cutoff Frequency:**

$$\omega_T = \frac{g_m}{C_{GC}} = \frac{\mu_n}{L^2}\left(V_{GS} - V_{TN}\right)$$

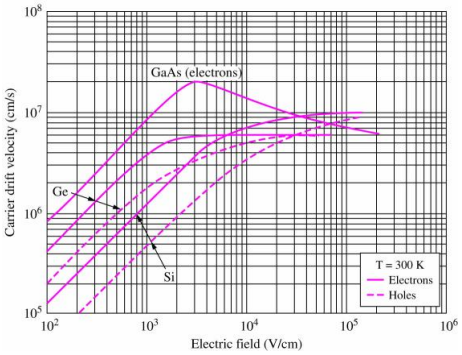
  - **f_T improves with square of channel length reduction**

Impact of Velocity Saturation

- **At low electric field, electron velocity is proportional to field**
- **At high electric field, the velocity reaches a maximum called saturation velocity, v_{SAT}**

$$i_D = \frac{C_{ox}^{"} W}{2}\left(v_{GS} - V_{TN}\right) v_{SAT}$$

- **The drain current is proportional to ($v_{GS} - V_{TN}$) rather than its square**
- **There are (many) other corrections to the basic model when the channel become very short**
  - **Interested, take EE130**



NMOSFET in OFF State

- We had previously assumed that there is no channel current when $v_{GS} < V_{TN}$. This is incorrect!
- As v_{GS} is reduced (toward 0 V) below V_{TN}, the potential barrier to carrier diffusion from the source into the channel is increased.
- The drain current I_D is limited by carrier diffusion into the channel, rather than by carrier drift through the channel.
- This is similar to the case of a PN junction diode!
  - I_D varies exponentially with the potential barrier height at the source, which varies directly with the channel potential.

Sub-Threshold Leakage Current

- In the depletion (sub-threshold) region of operation, the channel potential is capacitively coupled to the gate potential. A change in gate voltage (Δv_{GS}) results in a change in channel voltage (Δv_{CS}):

$$i_D \propto \exp\left(\frac{\Delta V_{CS}}{V_T}\right)$$ Similar to pn junction diode!

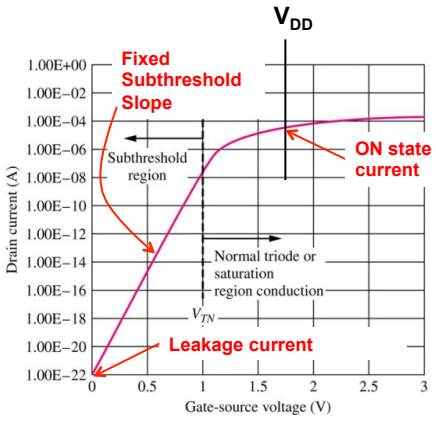
$$\Delta V_{CS} = \Delta V_{GS} \times \left(\frac{C_{ox}}{C_{ox} + C_{dep}}\right) \equiv \Delta V_{GS} / m, \qquad m = 1 + \frac{C_{dep}}{C_{ox}} > 1$$

Sub-threshold slope (also called sub-threshold swing):

$$S \equiv \left(\frac{d(\log_{10} I_{DS})}{dV_{GS}}\right)^{-1}$$

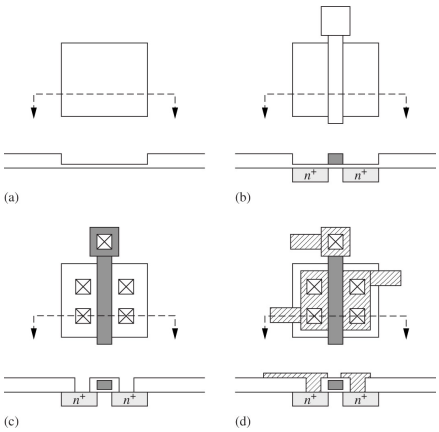
$$S = mV_T \ln(10) > 60\text{mV/dec}$$

MOS Transistor Scaling (cont.)



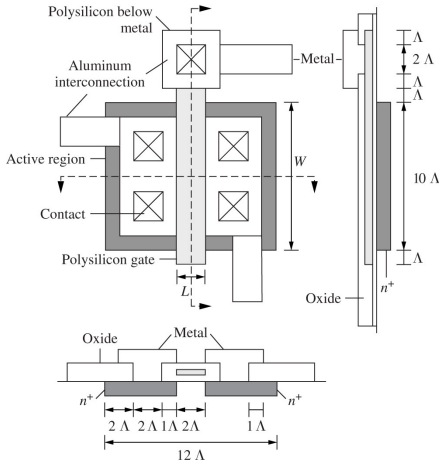
- Sub-threshold Conduction:
  - i_D decreases exponentially for $v_{GS} < V_{TN}$.
  - Reciprocal of the slope in mV/decade gives the turn-off rate for the MOSFET.
  - Fundamental limit of MOSFET sub-threshold slope: 60mV/decade

Mask Sequence Polysilicon-Gate Transistor



- Mask 1: Defines active area or thin oxide region of transistor
- Mask 2: Defines polysilicon gate of transistor, aligns to mask 1
- Mask 3: Delineates the contact window, aligns to mask 2.
- Mask 4: Delineates the metal pattern, aligns to mask 3.
- Channel region of transistor formed by intersection of first two mask layers. Source and Drain regions formed wherever mask 1 is not covered by mask 2

Basic Ground Rules for Layout

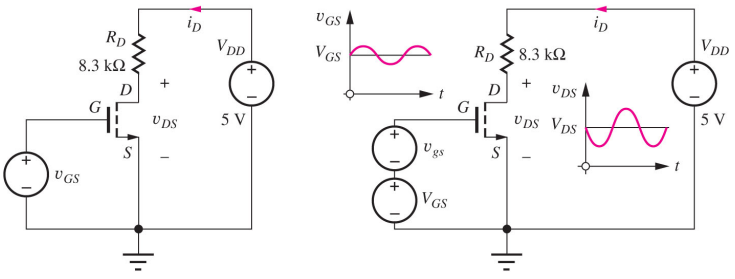


- **Design of large circuits can be simplified with simple rules**
- **Minimum feature size: F = 2 Λ**
- **Minimum alignment between different features: T = Λ**
- **Λ could be 1, 0.5, 0.25 μm, etc.**

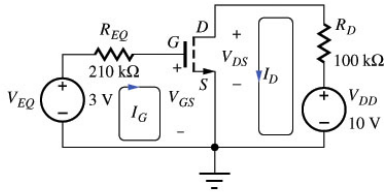
- **In this example:**
  - **W/L = 10Λ / 2Λ = 5**
  - **Transistor Area = 120 Λ²**

MOSFET Biasing

- **'Bias' sets the dc operating point.**
- **The 'signal' is actually comprised of relatively small changes in the voltages and/or currents.**
- **Remember (Total = dc + signal): $v_{GS} = V_{GS} + v_{gs}$ and $i_D = I_D + i_d$**



Bias Analysis - Example 1: Constant Gate-Source Voltage Biasing



Since $I_G = 0$,

$$V_{EQ} = I_G R_{EQ} + V_{GS} = V_{GS}$$

$$I_D = \frac{K_n}{2}\left(V_{GS} - V_{TN}\right)^2$$

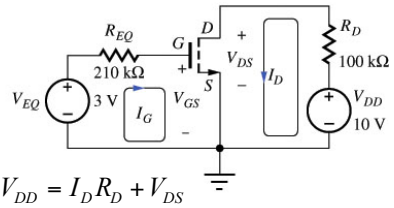
$$I_D = \frac{25x10^{-6}}{2}\frac{A}{V^2}\left(3-1\right)^2 V^2 = 50.0\ \mu A$$

$$V_{DD} = I_D R_D + V_{DS}$$

$$V_{DS} = 10V - \left(50\mu A\right)\left(100K\right) = 5.00\ V$$

- **Check: $V_{DS} > V_{GS}-V_{TN}$. Hence saturation region assumption is correct.**
- **Q-pt: (50.0 mA, 5.00 V) with V_{GS}= 3.00 V**
- **Discussion: The Q-point of this circuit is quite sensitive to changes in transistor characteristics, so it is not widely used.**

Bias Analysis Using Load Line



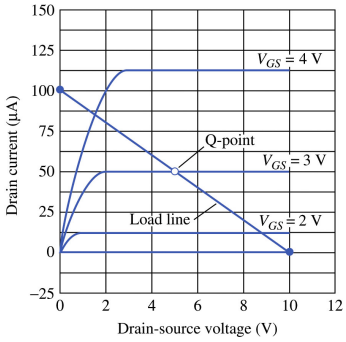
$$V_{DD} = I_D R_D + V_{DS}$$

$$10 = 10^5 I_D + V_{DS}$$

For V_{DS} = 0, I_D = 100 uA

For I_D = 0, V_{DS} = 10 V

Plotting the line on the transistor output characteristic yields Q-pt at intersection with V_{GS} = 3V device curve.



Check: The load line approach agrees with previous calculation.
Q-pt: (50.0 mA, 5.00 V) with V_{GS} = 3.00 V

Discussion: Q-pt is clearly in the saturation region. Graphical load line is good visual aid to see device operating region.

Bias Analysis - Constant Gate-Source Voltage Biasing with Channel-Length Modulation

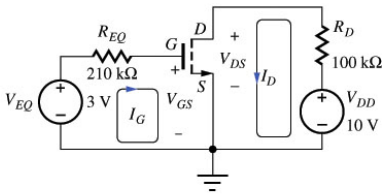
$$I_D = \frac{K_n}{2}\left(V_{GS} - V_{TN}\right)^2\left(1 + \lambda V_{DS}\right)$$

$$V_{DS} = V_{DD} - I_D R_D$$

$$V_{DS} = 10 - \frac{25x10^{-6}}{2}\left(10^5\right)\left(3-1\right)^2\left(1 + 0.02V_{DS}\right)$$

$$V_{DS} = 4.55\ V$$

$$I_D = \frac{25x10^{-6}}{2}\left(3-1\right)^2\left[1 + 0.02\left(4.55\right)\right] = 54.5\ \mu A$$

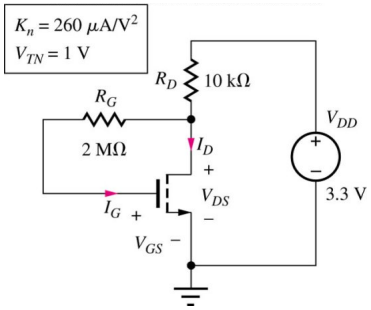


Check: $V_{DS} > V_{GS} - V_{TN}$. Hence the saturation region assumption is correct.

Q-pt: (54.5 mA, 4.55 V) with V_{GS} = 3.00 V

Discussion: The bias levels have changed by about 10% (54.5 µA vs 50 µA). Typically, component values will vary more than this, so there is little value in including λ effects in most circuits.

Bias Analysis - Example 6: Two-Resistor Feedback Biasing



Assumption: $I_G = I_B = 0$, transistor is saturated (since $V_{DS} = V_{GS}$)

Analysis: $V_{DS} = V_{DD} - I_D R_D$

$$V_{GS} = V_{DD} - \frac{K_n}{2}\left(V_{GS} - V_{TN}\right)^2 R_D$$

$$V_{GS} = 3.3 - \frac{2.6x10^{-4}}{2}\left(10^4\right)\left(V_{GS} - 1\right)^2$$

$$V_{GS} = -0.769\ V \text{ or } +2.00\ V$$

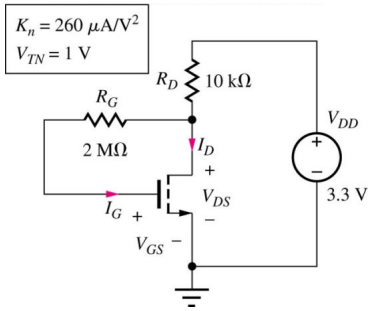
Since $V_{GS} < V_{TN}$ for V_{GS} = -0.769 V, the MOSFET would be cut-off,

$$\therefore V_{GS} = +2.00\text{ V} \text{ and } I_D = 130\ \mu A$$

$V_{DS} > V_{GS} - V_{TN}$. Hence saturation region assumption is correct.

Q-pt: (130 µA, 2.00 V)

Bias Analysis - Example 6: Two-Resistor Feedback Biasing



Assumption: $I_G = I_B = 0$, transistor is saturated (since $V_{DS} = V_{GS}$)

Analysis: $V_{DS} = V_{DD} - I_D R_D$

$$V_{GS} = V_{DD} - \frac{K_n}{2}\left(V_{GS} - V_{TN}\right)^2 R_D$$

$$V_{GS} = 3.3 - \frac{2.6x10^{-4}}{2}\left(10^4\right)\left(V_{GS} - 1\right)^2$$

$$V_{GS} = -0.769\ V \text{ or } +2.00\ V$$

Since $V_{GS} < V_{TN}$ for $V_{GS} = -0.769$ V, the MOSFET would be cut-off,

$$\therefore V_{GS} = +2.00\ \text{V} \text{ and } I_D = 130\ \mu A$$

$V_{DS} > V_{GS}-V_{TN}$. Hence saturation region assumption is correct.

Q-pt: (130 µA, 2.00 V)

Bias Analysis – Two-Resistor biasing for PMOS Transistor

Assumption: $I_G = I_B = 0$; transistor is saturated

Analysis:

$$V_{GS} - I_G R_G - V_{DS} = 0 \rightarrow V_{DS} = V_{GS}$$

$$V_{DD} + V_{DS} - I_D R_D = 0$$

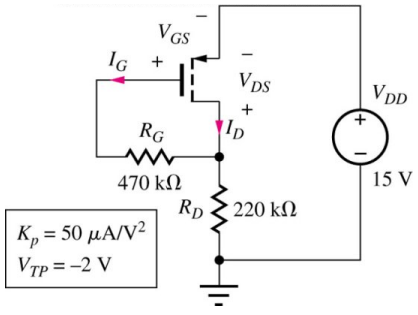
$$V_{DD} + V_{GS} - \frac{K_n}{2}\left(V_{GS} - V_{TP}\right)^2 R_D = 0$$

$$15 + V_{GS} - \left(2.2x10^5\right)\frac{5x10^{-5}}{2}\left(V_{GS} + 2\right)^2 = 0$$

$$V_{GS} = -0.369\ V \text{ or } -3.45\ V$$

Since $V_{GS} = -0.369 > V_{TP}$, $V_{GS} = -3.45\ V$

$$I_D = 52.5\ \mu A \quad \text{and} \quad V_{DS} = -3.45\ V$$



$$|V_{DS}| > |V_{GS} - V_{TP}|$$

Hence saturation assumption is correct.

Q-pt: (52.5 µA, -3.45 V)